

1 17. (twice amended) A method of fabricating a portion of a semiconductor device comprising:  
2 forming a gate structure on a substrate by:  
3 *B'* forming an insulating oxide layer on the substrate;  
4 depositing a nitride layer on the oxide layer; and  
5 depositing a polysilicon layer on the nitride layer; and  
6 reoxidizing the gate structure to form a layer of oxide over the gate structure.

1 18. (unchanged) The method of claim 17, wherein the depositing step includes depositing the nitride  
2 layer on the insulating oxide layer to a thickness from about 10 Å to about 50 Å.

1 19. (unchanged) The method of claim 17, wherein the reoxidizing step includes reoxidizing the gate  
2 structure to form an oxide layer from about 25 Å to about 500 Å thick.

1 20. (unchanged) The method of claim 17, further comprising:  
2 patterning the gate structure by selectively etching away portions of the insulating oxide,  
3 nitride and polysilicon layers to expose a portion of the substrate and form a peripheral edge around  
4 the gate structure; and  
5 exposing the substrate to an oxidizing ambient during reoxidation to oxidize the exposed  
6 portion of the substrate.

1 21. (unchanged) The method of claim 20, wherein the reoxidation causes an uplift in a peripheral  
2 portion of the nitride layer.

1 22. (unchanged) The method of claim 20, wherein the reoxidation causes an indentation in the  
2 substrate near the peripheral edge of the gate structure.

1 23. (unchanged) The method of claim 17, further comprising:  
2 prior to the reoxidizing step, forming source and drain regions in the substrate.

1 25. (unchanged) A method for fabricating a portion of a semiconductor device, comprising:  
2 forming an oxide gate layer on a surface of a substrate;  
3 forming a nitride layer on the oxide gate layer by depositing the nitride layer on the oxide  
4 gate layer;  
5 forming a polysilicon layer on the nitride layer;  
6 patterning the polysilicon and nitride layers to form a gate structure; and  
7 reoxidizing the gate structure to form a layer of oxide over the gate structure and on sidewalls  
8 of the gate structure.

1 46. (unchanged) An integrated circuit device comprising:  
2 a substrate;  
3 a gate structure, wherein the gate structure includes:  
4 a gate oxide layer on the substrate,  
5 a nitride layer on the gate oxide layer, and  
6 a polysilicon layer over the nitride layer;  
7 a channel region under the gate structure; and  
8 source/drain regions in the substrate adjacent the channel region.

1 47. (unchanged) The integrated circuit device of claim 46, wherein the nitride layer is from about  
2 10 Å to about 50 Å thick.

1 48. (unchanged) The integrated circuit device of claim 46, wherein the nitride layer is deposited over  
2 said gate oxide layer.

1 49. (unchanged) The integrated circuit device of claim 46, wherein the nitride layer is formed by  
2 nitrogen implantation to form an implanted area and by annealing of the implanted area.

1 50. (unchanged) The integrated circuit device of claim 46, wherein the gate structure has a  
2 peripheral edge and further including an uplift in portions of the nitride layer proximate the  
3 peripheral edge of the gate structure, the uplift caused by reoxidation of the gate structure, wherein  
4 asperities are absent from the polysilicon layer.

1 51. (unchanged) The integrated circuit device of claim 46, wherein the substrate has a surface and  
2 further including an indentation in the surface of the substrate located proximate to the peripheral  
3 edge of the gate structure, the indentation resulting from reoxidation of the gate structure.

1 52. (unchanged) The integrated circuit device of claim 46 further wherein the gate structure includes  
2 sidewall spacers located on each edge of the gate structure and lightly doped drain regions in the  
3 substrate below the sidewalls spacers.

1 53. (unchanged) The integrated circuit device of claim 46, wherein the substrate is a p-type substrate  
2 and wherein the source/drain regions are formed by implanting n-type impurities in the p-type  
3 substrate.

1 54. (unchanged) The integrated circuit device of claim 53, wherein the source/drain regions are  
2 implanted prior to reoxidation.

1 55. (unchanged) The integrated circuit device of claim 53, wherein the source/drain regions are  
2 implanted after oxidation.

1 56. (unchanged) The integrated circuit device of claim 46, wherein the channel region has a length  
2 not greater than 0.8  $\mu\text{m}$ .

1 57. (unchanged) The integrated circuit device of claim 46, wherein the gate oxide layer is not greater  
2 than 200 Å thick.

1 58. (unchanged) The method of claim 23, wherein a channel region beneath the gate structure  
2 between the source/drain regions has a length not greater than 0.8  $\mu\text{m}$ .

1 59. (unchanged) The method of claim 25, further comprising:  
2 forming the oxide gate layer to a thickness not greater than 200 Å.